WHAT IS CLAIMED IS:

1. A graphical profile map for integrated circuits on a substrate, the graphical profile map comprising a depiction of:
die placement boundaries for the integrated circuits on the substrate,
shot placement boundaries for the integrated circuits on the substrate, and
integrated circuit property information contours, where the contours are not limited to either of the die placement boundaries and the shot placement boundaries.

2. The graphical profile map of claim 1, wherein the integrated circuit property information is provided from a database of historical integrated circuit property information when a desired amount of historical integrated circuit property information is available, and when the desired amount of historical integrated circuit property information is not available, the integrated circuit property information is provided by programmable algorithms.

3. The graphical profile map of claim 2, wherein the programmable algorithms comprise modification algorithms and smoothing algorithms and the algorithms are implemented by at least one of manually by an engineer, automatedly by an intelligent agent, and automatedly by an intelligent script.

4. The graphical profile map of claim 1, wherein the graphical profile map is stored as an image file on a computer readable media.

5. The graphical profile map of claim 1, wherein the integrated circuit property information comprises composite integrated circuit property information for all processes that the integrated circuits have undergone.

6. The graphical profile map of claim 1, wherein the integrated circuit property information comprises integrated circuit property information for a selectable single process that the integrated circuits have undergone.

7. The graphical profile map of claim 1, wherein the integrated circuit property information comprises integrated circuit property information for a selectable subset of processes that the integrated circuits have undergone.

8. The graphical profile map of claim 1, wherein the integrated circuit property information is presented by representing different integrated circuit property information value ranges with different colors.

9. The graphical profile map of claim 1, wherein the integrated circuit property information comprises yield information.

10. The graphical profile map of claim 1, wherein the shot placement boundaries comprise a graphical shot grid representation.

11. The graphical profile map of claim 1, wherein the die placement boundaries comprise a graphical die grid representation.

12. The graphical profile map of claim 1, further comprising a graphical indication depicting an offset from a center of the substrate to a center of a closest unit of the shot placement boundaries.

13. A method of creating a graphical profile map for integrated circuits on a substrate, the method comprising:

assembling die placement information for the integrated circuits on the substrate,

displaying the die placement information as die placement boundaries on a representation of the substrate,

assembling shot placement information for the integrated circuits on the substrate,

displaying the shot placement information as shot placement boundaries on the representation of the substrate,

assembling integrated circuit property information for the integrated circuits on the substrate, and

displaying the integrated circuit property information as contours on the representation of the substrate, where the contours are not limited to either of the die placement boundaries and the shot placement boundaries.

14. The method of claim 13, wherein the step of assembling the integrated circuit property information comprises acquiring the integrated circuit property information from a database of historical integrated circuit property information when a desired amount of historical integrated circuit property information is available, and when the desired amount of historical integrated circuit property information is not available, generating integrated circuit property information with programmable algorithms.

15. The method of claim 14, wherein the programmable algorithms comprise modification algorithms and smoothing algorithms.

16. The method of claim 13, wherein the integrated circuit property information is presented by representing different integrated circuit property information value ranges with different colors.

17. The method of claim 13, further comprising a graphical indication depicting an offset from a center of the substrate to a center of a closest unit of the shot placement information.

18. A method of creating a graphical yield profile map for integrated circuits on a substrate, the method comprising:

assembling die grid information for the integrated circuits on the substrate,

displaying the die grid information as die grid boundaries on a representation of the substrate,

assembling shot grid information for the integrated circuits on the substrate,

displaying the shot grid information as shot grid boundaries on the representation of the substrate,

assembling yield information by location of the integrated circuits on the substrate, by acquiring the yield information from a database of historical yield information when a desired amount of historical yield information is available, and when the desired amount of historical yield information is not available, generating yield information with programmable algorithms,

displaying the yield information as contours on the representation of the substrate, where the contours are not limited to either of the die grid boundaries and the shot grid boundaries.

19. The method of claim 18, wherein the programmable algorithms comprise modification algorithms and smoothing algorithms.

20. The method of claim 18, wherein the yield information is presented by representing different yield value ranges with different colors.